IN THE CLAIMS

Following are the claims as currently pending for consideration.

1. (Original) An operating-system transparent method for sharing virtual address translations comprising:

accessing a virtual address translation; and

transparently identifying if the virtual address translation is sharable.

2. (Original) The method of Claim 1 further comprising

providing a first sharing indication if the virtual address translation is identified as sharable.

3. (Original) The method of Claim 2 further comprising

providing a second sharing indication if the virtual address translation is identified as not sharable.

4. (Original) The method of Claim 2 wherein the first sharing indication indicates a set of logical processes sharing the virtual address translation.

5. (Original) The method of Claim 3 wherein the second sharing indication indicates a private status for the virtual address translation.

6. (Original) The method of Claim 5 wherein the second sharing indication implicitly indicates a private status for the virtual address translation.

7. (Original) The method of Claim 5 wherein the first sharing indication indicates a shared status for the virtual address translation.

8. (Original) The method of Claim 7 wherein the second sharing indication implicitly indicates a shared status for the virtual address translation.

9-12. (Canceled)

13. (Original) A processing system providing operating-system transparent sharing of virtual address translations, the processing system comprising:

a first logical processor;

a second logical processor;

a storage location to store a virtual address translation; and

a control logic to access a first virtual address translation for the first logical processor in the storage location and to transparently produce a first sharing indication if the virtual address translation may be shared with the second logical processor.

14. (Original) The processing system of Claim 13 wherein the first logical processor and the second logical processor are located on the same die.

15. (Original) The processing system of Claim 14 wherein the first logical processor and the second logical processor support multithreading.

16. (Original) The processing system of Claim 13 wherein the virtual address translation is to provide the first and second logical processors access to a shared cache.

17. (Original) The processing system of Claim 16 wherein the sharing indication comprises a set of logical processors sharing the virtual address translation.

18. (Original) The processing system of Claim 16 wherein the shared cache stores data comprising executable instructions for the first and second logical processors.

19. (Original) The processing system of Claim 13 wherein the storage location to store the virtual address translation is further to store the first sharing indication if the virtual address translation may be shared.

20. (Original) An apparatus to provide operating-system transparent sharing of virtual address translations, the apparatus comprising:

a control logic to access a first virtual address translation for a first processor,

the control logic further to transparently provide a first sharing indication if the first virtual address translation may be shared with a second processor.

21. (Original) The apparatus of Claim 20 wherein the control logic comprises:

circuitry to provide a sharing indication to indicate that the virtual address translation translates a virtual address for the second processor.

22. (Original) The apparatus of Claim 20 wherein the control logic comprises:

a combination of circuitry and machine executable processes to compute data of a second virtual address translation for the second processor.

23. (Original) The apparatus of Claim 22 wherein the combination of circuitry and machine executable processes compare the computed data of the second virtual address translation to a corresponding data of the first virtual address translation to identify if the first virtual address translation may be shared with the second processor.

24. (Original) The apparatus of Claim 20 further comprising:

a translation lookaside buffer to store the virtual address translation for the first processor.

25. (Original) The apparatus of Claim 24 wherein the translation lookaside buffer is further to store the first sharing indication if the first virtual address translation may be shared with a second processor.

26. (Original) The apparatus of Claim 24 wherein the first virtual address translation is to provide the first and second processors access to a shared cache.

27. (Original) The apparatus of Claim 26 wherein the shared cache is accessed according to physical addresses.

28. (Original) The apparatus of Claim 20 wherein the control logic is further to provide a second sharing indication if the first virtual address translation may not be shared with the second processor.

29. (Original) The apparatus of Claim 28 wherein the first sharing indication, indicates a set of logical processes sharing the first virtual address translation.

30. (Original) The apparatus of Claim 28 wherein the second sharing indication, indicates a private status for the first virtual address translation.

31-35. (Canceled)

36. (Previously Presented) A multithreading processor comprising:

an address translation stage including a translation lookaside buffer having a plurality of entries to translate virtual addresses to physical addresses;

a first entry of the plurality of entries to translate a first virtual address for a first process;

a control logic comprising circuitry to identify a sharability of the first entry;

the control logic further to provide a first sharing indication to indicate if the first entry may be shared by a second process; and

a sharing indication field in the first entry to store the first sharing indication provided by the control logic.

37. (Previously Presented) The processor of Claim 36 wherein the sharing indication field indicates a set of processes that have been identified to share the first entry.

38. (Previously Presented) The processor of Claim 36 wherein the control logic comprises:

circuitry to provide a sharing indication to indicate that the first entry has an address space identifier data and a virtual address data of the second process.

39. (Previously Presented) The processor of Claim 38 wherein the control logic comprises:

a combination of circuitry and state machine executable processes to determine said address space identifier data and said virtual address data of a second virtual address translation for the second process and to compare them with the first entry.

40-46. (Canceled)